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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,961	03/30/2004	Fumio Hara	XA-10066	2879

181 7590 05/04/2006

MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
SONG, JASMINE	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,961	HARA ET AL.	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,9,10,14,16 and 19* is/are rejected.

7)☒ Claim(s) *6,8,11-13,15,17,18,20 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/30/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

2. The drawings filed on 03/30/2004 have been approved by the Examiner.

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Priority

4. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 04/14/2003. It is noted, however, that applicant has not filed a certified copy of the 2003-108603 application as required by 35 U.S.C. 119(b).

Information Disclosure Statement

5. The information disclosure statement (IDS) submitted on 03/30/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Title

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claim 16 is rejected under 35 U.S.C. 102(e) as being anticipated by Ayaki et al., US 6,553,476 B1

Regarding claim 16, Ayaki teaches that a memory device including: a nonvolatile memory (it is taught as a hard disk drive 1 in Fig.1); a buffer memory (it is taught as the buffer RAM 3 in Fig.1) having a higher access speed than the nonvolatile memory (since buffer RAM 3 is a temporary memory circuit for temporarily storing data, col.10,

lines 7-8, the interface circuit 2 in Fig.1 output data received from the buffer RAM 3 in response to the commands received from the external system such as a host computer, col.10, lines 19-23 and col.10, lines 1-3; using a buffer as a read ahead buffer for reading and writing data is will-known technique for increasing the data I/O rate of new high capacity HDD systems); and a control circuit (HDD control circuit 9 in Fig.1), wherein in response to a preread command inputted from the outside (col.23, lines 30-34), the control circuit creates a preread data management table that associates a logical address of preread data specified by the command (col.23, lines 37-46) and a buffer memory address (it is taught as buffer RAM 3) for storing the preread data (col.23, lines 37-42), and reads data specified by the command from the nonvolatile memory (Fig.12, it is taught as reads data specified by the preread command from disk apparatus 31) and stores the data in the buffer memory as preread data (Fig.12 and col.23, lines 37-40 and lines 49-51) so that the preread data stored in the buffer memory can be outputted to the outside (it is taught as a command requesting the transfer data size is issued to the disk apparatus and receives the amount of continuously readable data such as preread data amount, col.23, lines 61-63).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-5,7,9-10,14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ayaki et al., US 6,553,476 B1, in view of Magro., US 6,754,779 B1.

Regarding claim 1, Ayaki teaches that a memory device comprising:

a nonvolatile memory (it is taught as a hard disk drive 1 in Fig.1); a buffer memory (it is taught as the buffer RAM 3 in Fig.1) having a higher access speed than the nonvolatile memory (since buffer RAM 3 is a temporary memory circuit for temporarily storing data, col.10, lines 7-8, the interface circuit 2 in Fig.1 output data received from the buffer RAM 3 in response to the commands received from the external system such as a host computer, col.10, lines 19-23 and col.10, lines 1-3); and a control circuit (HDD control circuit 9 in Fig.1),

wherein the control circuit creates a preread data management table that associates a logical address of preread data (col.23, lines 37-46) specified by a preread command inputted from the outside (col.23, lines 30-34) and a buffer memory address (it is taught as buffer RAM 3) for storing the preread data (col.23, lines 37-42), reads data specified by the command (it is taught as the data specified by the preread command) from the nonvolatile memory (it is taught as hard disk drive, it is noticed that the configuration of the disk apparatus according to the fourth embodiment is substantially similar to that of the disk apparatus according to the first embodiment shown in Fig.1) and stores the data in the buffer memory as preread data (col.23, lines 37-42).

Avaki does not teach outputting corresponding preread data from the buffer memory when a logical address specified in a read command inputted from the outside matches a logical address associated by the preread data management table. Avaki teaches the read command is issued after the preread command for the same data (col.23, lines 57-58).

However, Magro teaches outputting corresponding preread data from the buffer memory (it is taught as outputting preread data from the data store 208; col.10, lines 43-47) when a logical address specified in a read command inputted from the outside (it is taught as the next requested data address from the read ahead buffer controller 62 on the PREFETCH_ADDR address bus, col.10, lines 35-43) matches a logical address associated by the preread data management table (it is taught as either the TAG_ADDR1 address register 802 or the address in the TAG_ADDR0 address register 804).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Magro into Ayaki's system such as outputting corresponding preread data from the buffer memory when a logical address specified in a read command inputted from the outside matches a logical address associated by the preread data management table because the prefetched data is stored locally, stored data matching a subsequent read request is provided to the requesting master in reduced, or zero wait states (In Magro, col.7, lines 29-32, col.10, lines 45-47 and col.12, lines 27-31) and avoiding unneeded and time consuming

accesses to the lower level memory (In Magro, col.8, lines 30-32 and col.10, lines 45-46).

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 2, Ayaki teaches that the preread command (col.23, lines 32-34) specifies preread data by a logical address (col.23, lines 37-40).

Regarding claim 3, Ayaki teaches that the preread command specifies preread data by a file name (col.24, lines 45-47).

Regarding claim 4, Ayaki teaches that the control circuit transfers preread data to the buffer memory (it is taught as reproduces the data and stores in the buffer RAM 3;col.23, lines 37-40) during execution of a preread command (it is taught as step 91 reproduces the data and stores the data is the one of the steps of Fig.15 which is a flowchart showing the operation of processing the preread command, col.23, lines 32-34).

Regarding claim 5, Ayaki teaches that the control circuit creates a preread data management table before transferring preread data to the buffer memory (it is taught as

reproduces the data based on the logic address and stored in the buffer RAM as preread data, since the logical address is associated with the preread data management table and the preread data management table include the management information such as a storage position which is the destination of the preread data, therefore, producing a preread data management table before transferring preread data to the buffer memory).

Regarding claim 7, Ayaki teaches that the preread data management table includes areas for storing a start logical address of preread data (according to the specification page 16, a logical address is a sector number of a file, which is taught as a frame number to be preread first, col.24, lines 45-49, it is the one of the preread parameters), a start memory address of an area storing the preread data (it is taught as a start address of a storage in the Buffer RAM 3, col.23, lines 45-48, it is another preread parameters), and a data count of the preread data (it is taught as the number of frames to be preread).

Regarding claim 9, Ayaki teaches that the preread data management table includes an area for holding a file name containing preread data (it is taught as the identifier of the file management information table for the file to be preread, col.24, lines 46-47).

Regarding claim 10, Ayaki teaches that the preread data management table includes an area for holding an access count of preread data (it is taught as the preread parameter: the number of frames to be preread).

Regarding claim 14, Ayaki teaches that a memory device including: a nonvolatile memory (it is taught as a hard disk drive 1 in Fig.1); a buffer memory (it is taught as the buffer RAM 3 in Fig.1) having a higher access speed than the nonvolatile memory (since buffer RAM 3 is a temporary memory circuit for temporarily storing data, col.10, lines 7-8, the interface circuit 2 in Fig.1 output data received from the buffer RAM 3 in response to the commands received from the external system such as a host computer, col.10, lines 19-23 and col.10, lines 1-3); and a control circuit (HDD control circuit 9 in Fig.1), wherein the control circuit consults rewritable preread data management tables that associate logical addresses of preread data (col.23, lines 37-46) and buffer memory addresses (it is taught as buffer RAM 3) for storing the preread data (col.23, lines 37-42).

Ayaki does not teach determining whether the buffer memory holds data specified by the command in response to a read command inputted from the outside, outputs data read from the buffer memory to the outside if the buffer memory holds the data, otherwise, outputs data read from the nonvolatile memory to the outside. Avaki teaches the read command is issued after the preread command for the same data (col.23, lines 57-58).

However, Magro teaches outputting corresponding preread data from the buffer memory (it is taught as outputting preread data from the data store 208; col.10, lines 43-47) when a logical address specified in a read command inputted from the outside (it is taught as the next requested data address from the read ahead buffer controller 62 on the PREFETCH_ADDR address bus, col.10, lines 35-43) matches a logical address associated by the preread data management table (it is taught as either the TAG_ADDR1 address register 802 or the address in the TAG_ADDR0 address register 804), otherwise, outputs data read from the nonvolatile memory (it is taught as outputting data read from the next lower level storage, col.8, lines 19-23 and col.10, lines 43-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Magro into Ayaki's system such as outputting corresponding preread data from the buffer memory when a logical address specified in a read command inputted from the outside compares and matches a logical address associated by the preread data management table, otherwise, outputting data read from the nonvolatile memory because the prefetched data is stored locally, stored data matching a subsequent read request is provided to the requesting master in reduced, or zero wait states (In Magro, col.2, lines 4-5; col.7, lines 29-32, col.10, lines 45-47 and col.12, lines 27-31) and performance of read operations is increased (In Magro, col.1, last line to col.2, lines 5).

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated

one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 19, Ayaki teaches the claimed invention (claim 16) as shown above, Ayaki does not teach that in response to a read command inputted from the outside, the control circuit consults the preread data management table to determine whether the buffer memory holds data specified by the command, and if the buffer memory holds the data, outputs data read from the buffer memory to the outside, otherwise, outputs data read from the nonvolatile memory to the outside. Avaki teaches the read command is issued after the preread command for the same data (col.23, lines 57-58).

However, Magro teaches outputting corresponding preread data from the buffer memory (it is taught as outputting preread data from the data store 208; col.10, lines 43-47) when a logical address specified in a read command inputted from the outside (it is taught as the next requested data address from the read ahead buffer controller 62 on the PREFETCH_ADDR address bus, col.10, lines 35-43) matches a logical address associated by the preread data management table (it is taught as either the TAG_ADDR1 address register 802 or the address in the TAG_ADDR0 address register 804), otherwise, outputs data read from the nonvolatile memory (it is taught as outputting data read from the next lower level storage, col.8, lines 19-23 and col.10, lines 43-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Magro into Ayaki's system such as outputting corresponding preread data from the buffer memory when a logical address specified in a read command inputted from the outside compares and matches a logical address associated by the preread data management table, otherwise, outputting data read from the nonvolatile memory because the prefetched data is stored locally, stored data matching a subsequent read request is provided to the requesting master in reduced, or zero wait states (In Magro, col.2, lines 4-5; col.7, lines 29-32, col.10, lines 45-47 and col.12, lines 27-31) and performance of read operations is increased (In Magro, col.1, last line to col.2, lines 5).

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Allowable Subject Matter

11. Claim 6,8,11-13,15,17-18 and 20-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record does not teach or suggest that the control circuit transfers preread data to the buffer memory in a command wait state after the termination of

execution of a preread command as claimed in claim 6 in combination with the other elements set forth in the claimed invention. Claim 8 is dependent on claim 6 and incorporated with the additional allowable subject matters.

The prior art of record does not teach or suggest that the control circuit searches for a buffer memory address infrequently accessed based on an access count held in the preread data management table and allocates an area of the located buffer memory address to anew area for storing preread data when no unused area for storing preread data is present in the buffer memory as claimed in claim 11 in combination with the other elements set forth in the claimed invention.

The prior art of record does not teach or suggest that the control circuit preread data management table to a preread data management table save area of the nonvolatile memory in a predetermined timing as claimed in claim 12 in combination with the other elements set forth in the claimed invention. Claim 13 is dependent on claim 12 and incorporated with the additional allowable subject matters.

The prior art of record does not teach or suggest that the control circuit reads preread data management tables from the nonvolatile memory in response to power on, and transfers preread data located by the read preread data management tables from the nonvolatile memory to the buffer memory as claimed in claim 15 in combination with the other elements set forth in the claimed invention.

The prior art of record does not teach or suggest that the control circuit allows selection between permission and inhibition of overwriting to areas already holding preread data when no unused area for storing preread data is present in the buffer

memory as claimed in claim 17 in combination with the other elements set forth in the claimed invention. Claim 18 is dependent on claim 17 and incorporated with the additional allowable subject matters.

The prior art of record does not teach or suggest that the control circuit consults the preread data management table to determine whether the buffer memory holds data of a write address specified by the command, and updates the data of the buffer memory by write data along with data of the nonvolatile memory if the buffer memory holds the data in response to a write command as claimed in claims 20 and 21 in combination with the other elements set forth in the claimed invention.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Uchihori	US 6,516,389 B1
Hirao et al	US 2003/0041214 A1
Shibazaki et al	US 6625712 B2
Tobita et al	US 5973964
Takaichi	US 6965967 B2

13. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

14. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 571-272-4213. The examiner can normally be reached on 7:30-5:30 (first Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jasmine Song

Patent Examiner

April 28, 2006